

Design and characterization of micromachined sensor array integrated with CMOS based optical readout

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ARTICLE INFO

Article history:

Received 19 April 2013

Received in revised form 13 October 2013

Accepted 14 October 2013

Available online 28 October 2013

Keywords:

Thermal detector

MEMS & CMOS integration

Optical readout

Diffraction grating

Fourier optics

ABSTRACT

This paper reports a micro electro-mechanical system (MEMS) based sensor array integrated with CMOS-based optical readout. The integrated architecture has several unique features. MEMS devices are passive and there are no electrical connections to the MEMS sensor array. Thus, the architecture is scalable to large array formats for parallel measurement applications and can even be made as a disposable cartridge in the future using self-aligning features. A CMOS-based readout integrated circuit (ROIC) is integrated to the MEMS chip. Via holes are defined on ROIC by customized post-processing and MEMS chip is thinned down by a grinding process to enable integrated optical readout. A diffraction grating interferometer-based optical readout is realized by pixel-level illumination of the MEMS chip through the via holes and by capturing the reflected light using a photodetector array on the CMOS chip. A model for the optical readout principle has been developed using Fourier optics.

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1. Introduction

Integration of MEMS devices with CMOS electronics in a small package enables many key features such as large array operation, low cost, and better control of environment. Integration of optical MEMS devices with customized CMOS has been demonstrated for optical microphones [1] and accelerometers [2]. These are either single devices or a small array of a few devices. Yet, integration of large devices is still challenging and poses a significant bottleneck for current technology.

This paper reports a MEMS-based sensor array integrated with CMOS-based optical readout [3] as shown in Fig. 1a. The MEMS devices in Fig. 1a are electrically passive and free of electrical connections. This enables large array formation for parallel measurement applications. Furthermore, different passive MEMS chips can be used with the same CMOS chip that allows configuring MEMS chips as disposable cartridges. Besides, MEMS chip can be operated in ambient, vacuum, or aqueous environments. A customized post-processing flow is developed to integrate the MEMS chip with CMOS-based readout integrated circuit. Via holes are defined on ROIC to enable integrated optical readout. The chips are aligned with about 1 μm accuracy using self-alignment marks.

It is possible to design sensors, different sensing modalities, and sensitivities on the same array for various applications. Currently, the sensor platform is optimized for thermal imaging applications. The MEMS devices presented in this paper are suspended membranes connected to a transparent substrate via bimaterial and thermal isolation legs. Bimaterial legs that are made of materials with different coefficients of thermal expansion deflect when exposed to thermal input while thermal isolation legs prevent heat dissipation towards the substrate [4–9]. Mechanical deflection is detected optically with sub-nm precision using a pixel-level diffraction grating interferometer [10–13] as illustrated in Fig. 1b. Light reflects off of the membrane interferes with light reflects off of the diffraction gratings embedded under each device. Since the movable reflector, i.e. the membrane, and the reference reflector, i.e. diffraction grating, lay on the same substrate, the readout beam is immune to environmental vibration.

2. MEMS sensor design

MEMS sensor has seven operational structures: transparent substrate, metal diffraction gratings, membrane, infrared (IR) absorber, bimaterial legs, isolation legs, and top reflector as shown in Fig. 2a. A thin metal layer deposited on top of the membrane is used as the IR absorber. The transparent substrate and diffraction gratings are not labeled in the figure since these structures are below the membrane. Incident IR radiation is absorbed by a thin film metal lying on

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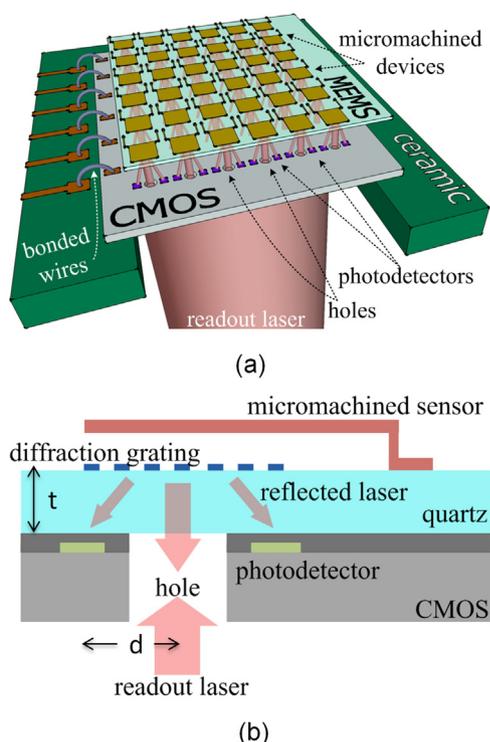


Fig. 1. (a) Side view of one sensor. (b) Schematic of the integrated device.

top of the suspended membrane. Induced temperature load due to absorbed radiation bends the bimaterial legs, which are composed of two materials with different coefficients of thermal expansion. Bimaterial legs are connected to the substrate through isolation legs that provides thermal isolation. Bending on bimaterial legs modulates the gap height between the substrate and the detector membrane. The change in gap is detected by optical means a diffraction grating based interferometer. These structures are illuminated using a laser beam from backside through the transparent substrate as shown in Fig. 1b. The reflected light goes into diffraction orders determined by the diffraction grating. The intensity of light in diffraction orders is modulated by the gap due to interference. The intensity of 1st diffraction order is monitored using a detector located under each MEMS device. Thus, a thermal map of the target is generated. Fig. 2b shows microscope image of individual devices with thicknesses of 400 nm parylene and 200 nm titanium.

The pixels are $35\ \mu\text{m}$ in pitch, and the bimaterial legs of the pixels are $25\ \mu\text{m}$ in length for each side of the pixel. The arrays are

fabricated in 64×64 array format. The structures are fabricated on a pyrex wafer using a four-mask process. Parylene provides a compliant mechanical support layer and is a good thermal isolator. The CTE (coefficient of thermal expansion) of the parylene is $35 \times 10^{-6}\ \text{K}^{-1}$ and the CTE of the titanium is $8.6 \times 10^{-6}\ \text{K}^{-1}$ [9]. Therefore, bimaterial legs are made of a combination of parylene with titanium that forms a good thermal mismatch pair. Reflector at the top of the body is made of titanium, patterned with the same mask. The fabrication steps of the parylene/titanium sensor arrays are given in Fig. 3.

Fabrication process is summarized in seven steps. In the 1st step, 100 nm of titanium layer is patterned as diffraction gratings on a pyrex wafer by using lift-off process. In the 2nd step, after coating the photoresist as a sacrificial layer, a photolithography step was performed to define the anchors. After defining the anchors, parylene C is deposited onto wafers as the structural material as a 3rd step. 4th step includes the deposition and patterning of titanium. In the 5th step etching of the parylene layer to define the isolation legs and absorption pads is performed. Release with resist remover and critical point dryer is the 6th step of the fabrication. Lastly, a titanium thin film is deposited as the absorber layer. The MEMS devices given in Fig. 2 are fabricated successfully according to the given fabrication steps.

3. CMOS-based optical readout

Deflection of individual devices in the array is measured using optical methods. Optical readout eliminates the need of electrical interconnects on pixels. So, the devices are free of detrimental effects of joule heating due to electrical bias and thermal crosstalk. Moreover, optical readout improves the sensitivity as it offers sub-nanometer resolution for the detection of the deflection of individual pixels simultaneously. Pixel-level interferometers are formed by blanket illumination of the entire focal plane array (FPA) using a single laser source. Reflected light from the individual devices that propagates in first diffraction order is imaged onto a 2D visible detector array.

3.1. CMOS characterization and post-processing

MEMS chip is integrated with a compatible CMOS ROIC chip to develop a compact and optimized sensing platform. CMOS chip including low power trans-impedance amplifiers, noise cancellation circuits, analog multiplexers, and decoders is designed and fabricated using a standard $0.18\ \mu\text{m}$ CMOS process. Fig. 4 shows ROIC chip that contains an array of holes and photodiodes to be aligned with MEMS devices. The orange box in Fig. 4 illustrates single pixel readout part of CMOS ROIC that includes one hole for

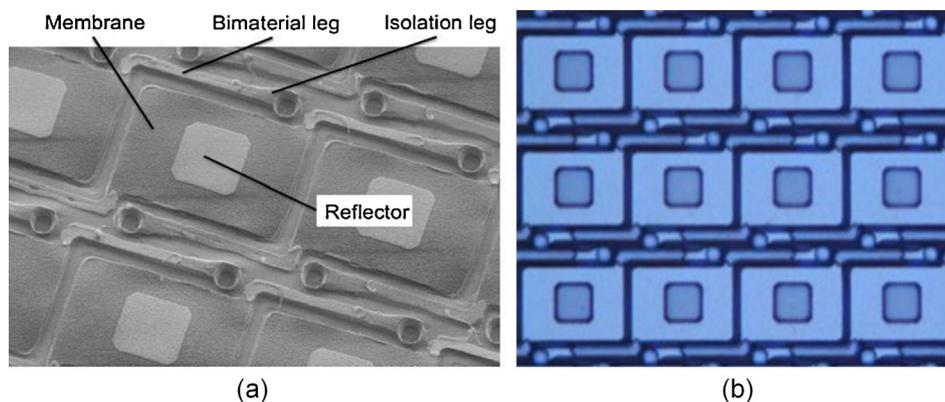


Fig. 2. (a) SEM pictures of $35\ \mu\text{m} \times 35\ \mu\text{m}$ MEMS sensors. (b) Microscope image of a larger array.

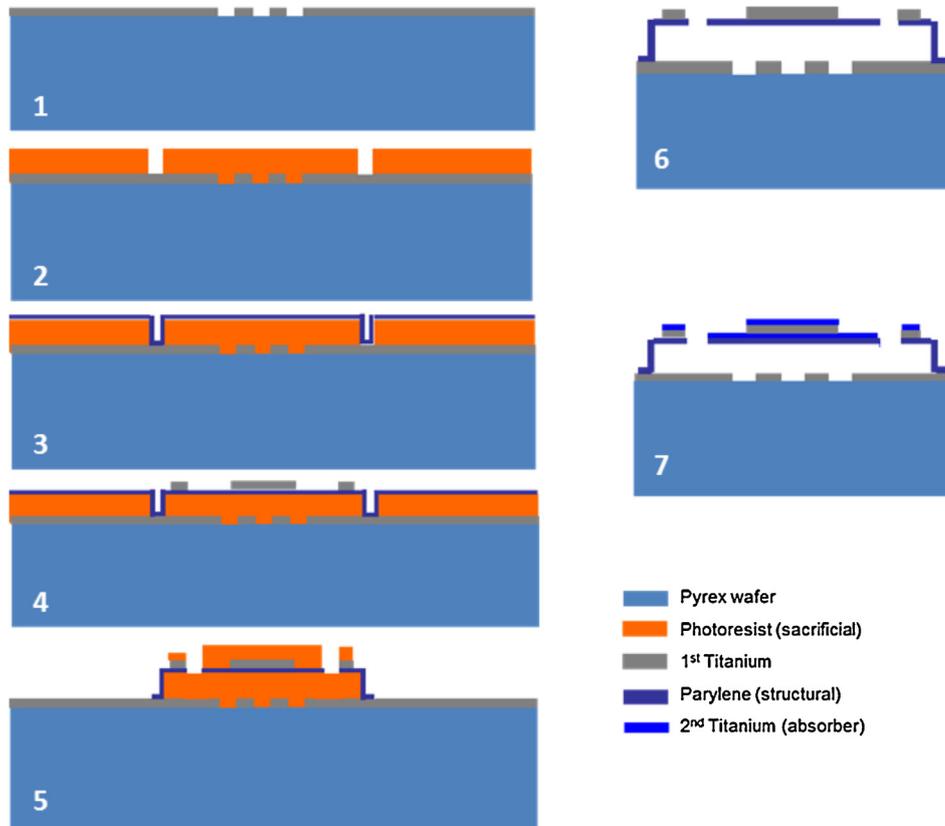


Fig. 3. Fabrication steps of Parylene/Ti sensor array.

incident beam and two photodiodes for ± 1 st diffraction orders. Holes provide optical access to the MEMS chip from backside and the photodiodes are located with respect to the reflectors of the IR sensors. Thus, the reflectors on the IR sensor should be aligned with the holes on the IC chip.

CMOS chip is fabricated with a thickness of 280 μm without the holes. In order to make the MEMS and CMOS compatible for the integration, post-processing is required. Fig. 5 shows the details of the CMOS chip after post-processing steps. Holes on CMOS chip are defined using a customized post-processing fabrication step. Top Al metal having hexagonal openings with 10 μm diameter is used as the etching mask for dielectric and Si etching. The dry-film lithography is used only to protect the I/O pads and the circuitry. First,

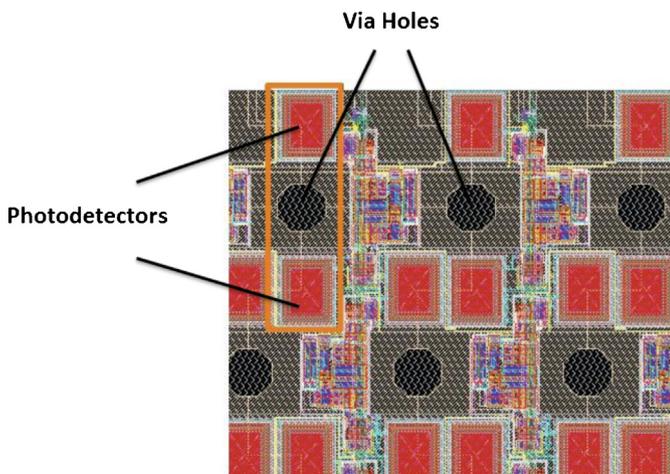


Fig. 4. CMOS ROIC, photodetector, and hole configuration.

the chips are thinned down to 100 μm with the grinding tool, while the initial thickness is 280 μm . After an O_2 plasma cleaning step, the chips are placed on a dummy Si wafer with 200 nm sputtered Al film. Then, 40 μm thick dry film is laminated and patterned. After the photolithography steps, about 11 μm of BEOL (back end of line) dielectric layers are etched by using dry etcher. Then, 100 μm of Si substrate is etched by DRIE. Finally, the CMOS top metal (860 nm thick) is cleaned in dry etcher. After the etching processes, the dry-film resist is stripped by using a resist stripper. The details of the process are explained in [14]. The diameter of via holes is 10 μm that is compatible with the size of the MEMS sensor. There are two photodetectors next to a hole for one MEMS device in the array to monitor light at +1st and -1st diffraction orders.

Furthermore, a graphical user interface is designed for the tests of readout circuit. The desired photodetector can be selected, duty cycle of the laser can be modulated, and the output voltages for different duty cycle ratios can be read and saved by using this interface. Photodetectors are individually addressable and the photo-responsivity is measured as 0.163 A/W as shown in Fig. 6. This figure shows single photodetector current with respect to different incidence laser power. For the characterization, CMOS chip was illuminated using a red laser and a mechanical chopper was used to vary the intensity of incident light.

3.2. Diffraction calculations

MEMS die post-processing is another important step before the integration. Optimal pyrex wafer thickness is computed using Fourier optics theory. MEMS dies are grinded to the required thickness before integration with the CMOS. The array of sensors is fabricated on a standard pyrex wafer with a thickness of 525 μm .

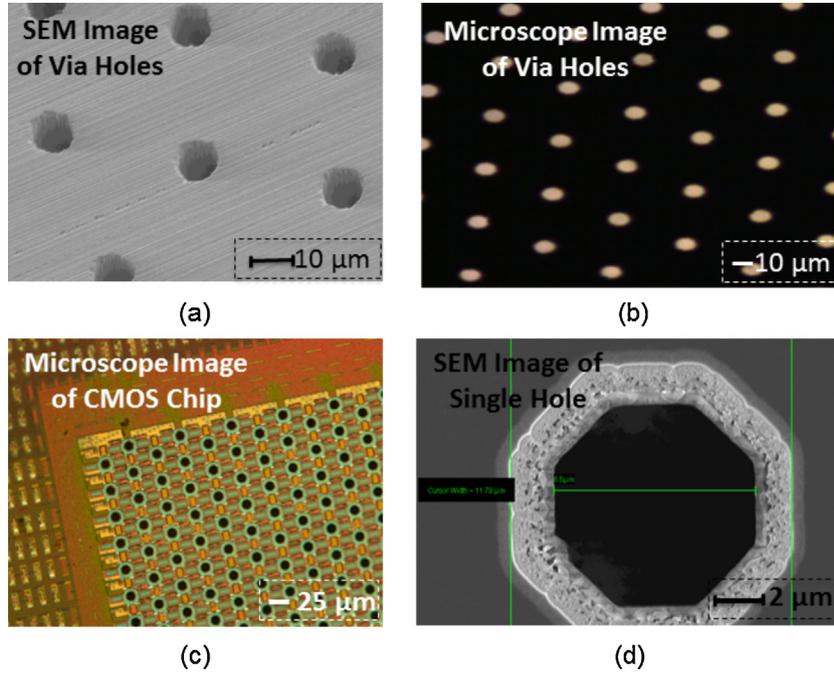


Fig. 5. (a) SEM image of backside of CMOS. (b) Microscope image showing the light transmission through via holes. (c) Microscope image of post-processed CMOS chip with via holes. (d) SEM image of a single hole from backside of CMOS.

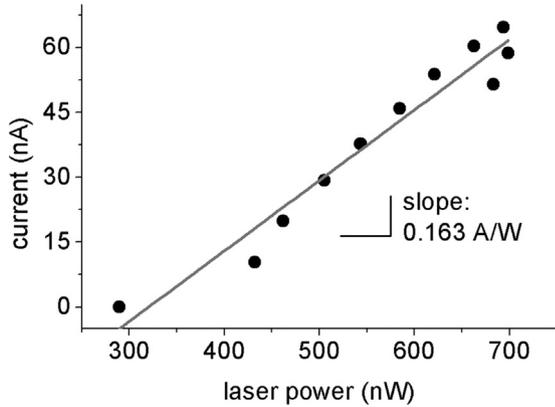


Fig. 6. CMOS characterization data.

The distance between the photodetectors ($2d$) is determined by the thickness (t) (see Fig. 1) as shown in Eqs. (1) and (2).

$$\theta_m = \sin^{-1} \left(\frac{m (\lambda / n_{pyrex})}{\Lambda} \right) - \sin \theta_i \tag{1}$$

$$t = d \cot(\theta_m) \tag{2}$$

θ_i : The angle of the incident light. m : Diffraction order (Integer). n_{pyrex} : Refractive index of pyrex. λ : Wavelength. Λ : Grating period. θ_m : The angle of the diffracted light. d : The distance between the center of the hole and a single photodiode. t : Thickness of the MEMS.

The period of diffraction gratings is $4 \mu\text{m}$. Normal incidence ($\theta_i = 0$) and a red laser with $\lambda = 635 \text{ nm}$ is assumed for the calculation. The distance between the center of the hole and the center of the photodiode (d) is $17 \mu\text{m}$. The photodiodes are $14 \mu\text{m} \times 14 \mu\text{m}$, the diameter of the hole is $10 \mu\text{m}$ and the length of guard bands at the same axis is $5 \mu\text{m}$ for both sides. For this configuration MEMS die should be grinded to $156 \mu\text{m}$.

A detailed model based on Fourier optics simulations has been developed to predict the distribution of intensities at the plane of photodetectors. Beam propagation simulations have been performed using the calculated thickness value and the given parameters. Input of the simulator is a uniform circular beam with a diameter of $10 \mu\text{m}$ as defined by the via hole at the backside of the pyrex wafer. The 2D beam profile at the plane of diffraction grating is obtained by propagating the input beam for a thickness of $t = 156 \mu\text{m}$ through grinded pyrex wafer as shown in Fig. 7a. Then the beam is propagated through the diffraction gratings to the movable reflector and the reflected light is propagated back to the detector plane. The 2D beam profile at the photo-detector (PD) plane is illustrated in Fig. 7b. The red squares indicate the location of the photo-detectors. The power going into ± 1 st diffraction orders is captured well with the current design.

The intensity of light at the photodetector plane at $y = 0$ is shown in Fig. 7c. The model verifies that the beams are well separated at the PD plane indicating a better signal quality.

4. MEMS and CMOS integration

MEMS and CMOS chips are aligned with $1 \mu\text{m}$ accuracy. This alignment accuracy ensures proper operation of relatively small photodiodes. Two alignment marks are added on both MEMS sensor and CMOS chip to facilitate the alignment process. The alignment marks are placed on top and bottom of the arrays to avoid rotation errors. A close-up detail of the integrated MEMS and CMOS chip placement is given in Fig. 8. A customized setup has been built for the alignment. The setup allows four degrees-of-freedom (three translational and one rotational) movement for the chips under a microscope.

An experimental setup is presented in Fig. 9 to characterize the integrated system using different inputs. An integrated device was illuminated using a pulsed laser beam with a wavelength of 635 nm . Response of the device to the pulsed laser beam corresponds to the dynamic range set by the power of the laser. Next, a small fan was placed about 50 cm in front of the MEMS device to test the system for a pressure wave input. The read out laser was

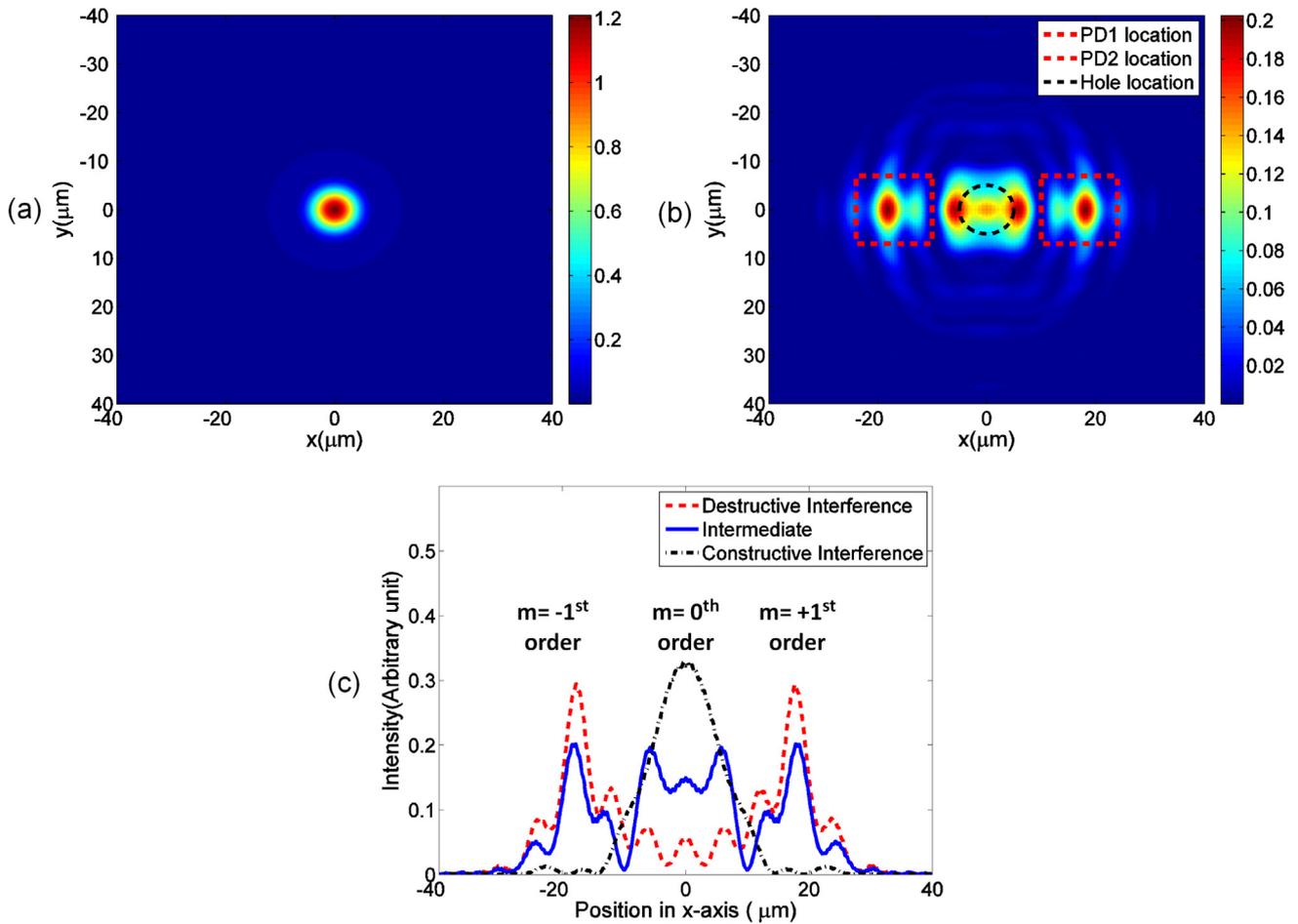


Fig. 7. (a) The propagated beam at the grating plane. (b) The diffraction orders at the photo-detector(PD) plane for 2 μm gap. (c) The cross section of the beam at the PD plane for three different gap values.

ON continuously while the fan was turned ON and OFF during this experiment. In addition, the response of the integration device was measured for a thermal load. A soldering iron heated at 150 °C was placed within the vicinity of the MEMS chip. The soldering iron was moved towards and away from the device during the experiment.

Fig. 10 shows a typical time traces of an exemplary pixel on the array for three different tests mentioned in Fig. 9. The outputs are normalized according to the response of the modulated laser. Normalized curves show the relative responses of the integrated device to different types of inputs. Nevertheless, the insets in Fig. 10 show that the system is capable of resolving the changes in the

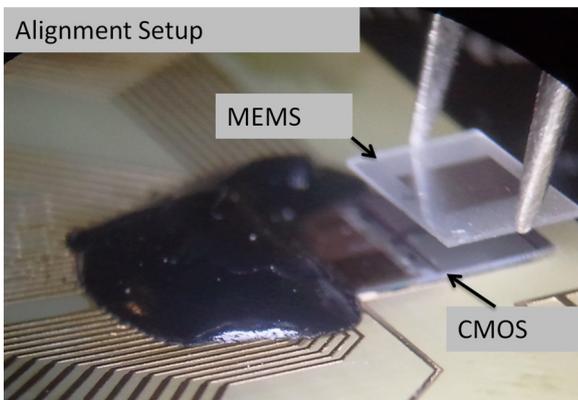


Fig. 8. Photograph of the alignment setup.

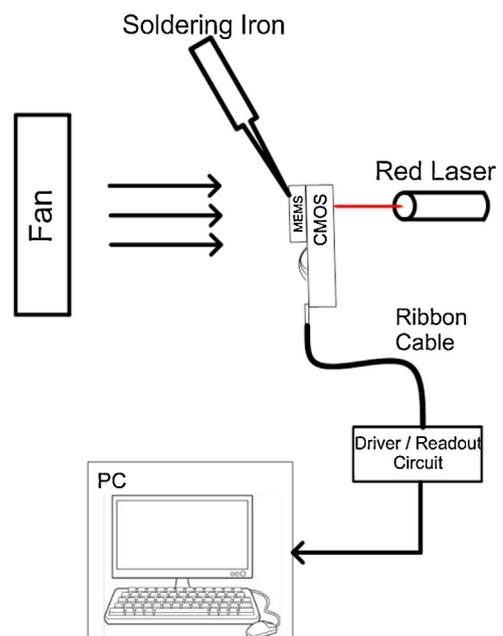


Fig. 9. Experimental setup to test the integrated system.

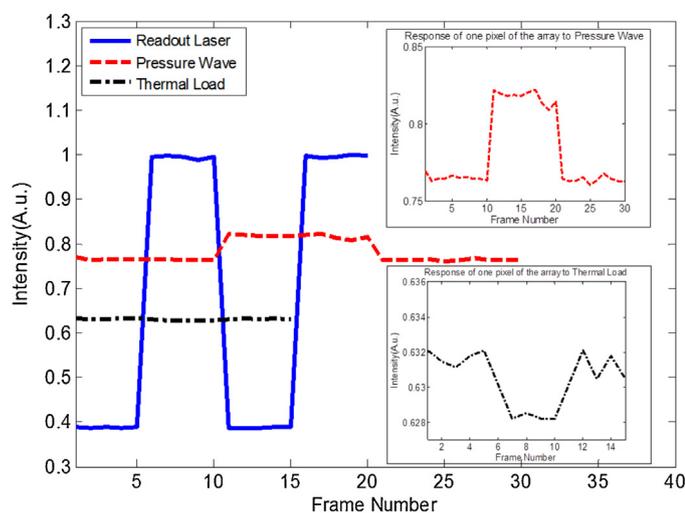


Fig. 10. Experimental characterization of the integrated system.

Table 1
System noise sources and NETD values.

Noise sources	NETD (10 bit) [mK]	NETD (12 bit) [mK]
NETD _{BF} (background fluctuation noise)	2.35	2.35
NETD _{TF} (thermal fluctuation noise)	4.16	4.16
NETD _{TM} (thermo-mechanical noise)	20.62	20.62
NETD _{OR} (optical readout noise)	809.18	202.29
NETD _{Total} (total noise)	809.45	202.4

inputs, indicating a successful integration of the CMOS chip with the MEMS.

The sensor array is developed mainly for IR imaging. The performance of the system is evaluated based on the NETD (noise equivalent temperature difference) that indicates the smallest detectable temperature difference at the target [4]. Table 1 shows the components of the NETD values for 10-bit and 12-bit readout electronics. The current performance is limited by the readout electronics and further improvement is possible using higher resolution electronics.

Several performance metrics are characterized, calculated or assumed for the NETD calculations. Experimentally measured thermo-mechanical sensitivity of 5 nm/K is used for the NETD calculations. The fill factor of the array is 60%, the detection bandwidth of the system is 30 Hz, $f\#$ of the IR system is 1. Thermal conductivity of a single MEMS pixel is calculated as 14×10^{-9} W/K for our system. Transmittance of the IR system (8–12 μm) is assumed 90%.

5. Conclusions

In this paper a MEMS sensor array platform integrated with CMOS-based optical readout is presented. The presented architecture is proposed as a sensor array for various applications. Optical readout capability without the need for electrical connections to the MEMS chip and simple integration to ROIC enables utilization of disposable and customized MEMS sensor arrays. Currently, the sensor platform is optimized for thermal imaging by designing a proper MEMS chip. Eliminating electrical connections on MEMS devices eliminate detrimental effects such as Joule heating and cross-talk. Interferometer-based optical readout improves the sensitivity of the integrated system. A successful integration is realized by post-processing the CMOS and the MEMS devices. A model based on Fourier optics simulations is presented. In this process, MEMS and CMOS are optimized and processed separately, improving the yield of the overall process. The system is tested for functionality using

pressure load and thermal load, and produced a response that was clearly detectable.

Acknowledgment

This work is funded by <gs1>AselsanInc (Turkey)</gs1>. R.B.E acknowledges support from TUBITAK scholarship for graduate studies.

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Ulas Adiyana received the B.Sc. degree in telecommunication engineering from Istanbul Technical University (ITU), Turkey, in 2007 and M.Sc. degree in electronic and communication engineering from the same university in 2010. His M.Sc. Thesis was about imaging 2-D buried objects. He was studying forward and inverse models of electromagnetic scattering from layered media. He is a Ph.D candidate in electrical engineering in Koc University. He is currently a member of OML research group. He is studying in the MOEMS thermal imaging project. His research interests are Fourier optics, uncooled infrared thermo-mechanical microsystems, and optical readout systems for thermal imaging.

Sevil Zeynep Lulec received her B.Sc. degree from Middle East Technical University, Ankara, Turkey, in 2008, and MS degree from École Polytechnique Fédérale de Lausanne, Switzerland, in 2010 both in Electrical and Electronics Engineering. She worked at Koc University, Optical Microsystems Laboratory, Istanbul, Turkey, and METU-MEMS Research and Application Center, Ankara, Turkey as Research Engineer. She is currently pursuing her Ph.D degree in Electronics Engineering at University of Toronto, Canada. Her research interests include analog and mixed signal IC design, MEMS modeling, and plasmonic integrated IR imaging. Mrs. Lulec was also recipient of the ADI Outstanding Student Designer Award (2013).

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Yuksel Temiz received his B.Sc. and M.Sc. degrees in Electrical and Electronics Engineering from Middle East Technical University (METU), Turkey, in 2005 and 2007, respectively, as the valedictorian. From 2005 to 2007, he worked as a research assistant at METU MEMS-VLSI Research Group, where he studied on readout and control electronics for MEMS inertial sensors. He received his Ph.D. degree in Microsystems and Microelectronics from Swiss Federal Institute of Technology in Lausanne (EPFL), in 2012. In his Ph.D. studies at Microelectronic Systems Laboratory (LSM) and Laboratory of Life Science Electronics (CLSE), he worked on the development of biosensor arrays in 3D-integration technology. He has developed chip-level post-CMOS processing techniques for TSV fabrication and chip-to-chip integration, and introduced an innovative biosensor system allowing the disposability of the microelectrode array and reusability of the electronics. He is currently a post-doctoral researcher in Nanofabrication and Experimental Bioscience groups at IBM Research-Zurich (Switzerland). His main research interests are 3D-IC technology, microfabrication technologies, microfluidics and interface electronics.

Yusuf Leblebici received the B.Sc. and M.Sc. degrees in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign (UIUC), in 1990. Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000-2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, he is a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the co-author of six textbooks, namely, *Hot-Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers, 1993), *CMOS Digital Integrated Circuits: Analysis and Design* (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), *CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications* (Springer, 2007), *Fundamentals of High Frequency CMOS Analog Integrated Circuits* (Cambridge University Press, 2009), *Nanosystems Design and Technology* (Springer, 2009), and *Extreme Low-Power Mixed Signal IC*

Design: Subthreshold Source-Coupled Circuits (Springer, 2011), as well as more than 300 articles published in various journals and conferences. Dr. Leblebici has served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (II) and IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He has also served as the general co-chair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference (ESSCIRC/ESSDERC). He is a Fellow of IEEE since 2010, and he has been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.

Hamdi Torun is an assistant professor at the Department of Electrical and Electronics Engineering and affiliated with the Center for Life Sciences and Technologies at Boğaziçi University, Istanbul, Turkey. He received his B.Sc. degree from Middle East Technical University, Ankara, Turkey, in 2003, his M.S. degree from Koç University, Istanbul, Turkey, in 2005, and his Ph.D. degree from the Georgia Institute of Technology, Atlanta, USA in 2009, all in electrical engineering. He was a postdoctoral fellow in the Department of Mechanical Engineering, Georgia Institute of Technology during 2009–2010. His research expertise is in development of microsystems for biomedical applications.

Hakan Urey received the B.Sc. degree from Middle East Technical University, Ankara, in 1992, and M.Sc. and Ph.D. degrees from Georgia Institute of Technology in 1996 and in 1997, all in Electrical Engineering. After completing his Ph.D, he joined Microvision Inc.-Seattle as Research Engineer and he played a key role in the development of the Retinal Scanning Display technology. He was the Principal System Engineer when he left Microvision to join the faculty of engineering at Koç University in 2001. He was promoted to Associate Professor in 2007 and Professor in 2010.

He published about 50 journals and 100 international conference papers, 7 edited books, 4 book chapters, and has more than 25 issued and several pending patents. His research interests are in the area of optical MEMS, micro-optics and optical system design, 2D/3D display and imaging systems, and biosensors. He is a member of SPIE, IEEE, and OSA.

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